present invention [emphasis added]." Applicants respectfully point out that Fig. 1A represents many different embodiments, including embodiments having all of the switches shown, and (as correctly identified by the examiner) embodiments having a subset of the switches shown. Applicants are not aware of any authority, (statutory, administrative, or otherwise), stating that a drawing is limited to a single embodiment of the invention. In the event of a continuing objection to the drawings, applicants respectfully request that some authority be cited in support of the examiner's position that the drawing should be limited to a single embodiment.

The office action also states that "[i]t is ... not clear what voltage the common node 168 is supposed to be at in Fig. 1A." Applicants respectfully submit that common node 168 is not necessarily supposed to be at any particular voltage, and that there is no requirement that the drawing be labeled with a voltage value. Accordingly, applicants believe that this objection to the drawings should be withdrawn.

Applicants acknowledge that the objections to the drawing will not be held in abeyance, and that the office action has requested that proposed drawing corrections or corrected drawings be submitted in order to avoid abandonment. Applicants believe that the above remarks are fully responsive to the drawing objections presented in the office action, and that the drawing objections have been overcome. Accordingly, no drawings are included with this response.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1, 8, and 12, and addition of new claims 29-34. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Amended) A comparator unit comprising:

a first amplifier stage including a differential amplifier having a pair of input nodes and a pair of output nodes, a switch connected across the pair of output nodes, and a non-linear load connected across the pair of output nodes; and

a second amplifier stage coupled to the pair of output nodes[.], the second amplifier stage

Q7, Q8 Q9, Q10

including an input pair of isolated gate field-effect transistors and a cross-coupled pair of isolated gate field-effect transistors, wherein each of the cross-coupled pair of isolated gate field-effect transistors is coupled in parallel with a corresponding one of the input pair of isolated gate field-effect transistors.

8. (Amended) The comparator unit of claim [2] 7, wherein the second amplifier stage includes a pair of second stage output nodes and a switch connected across the pair of second stage output nodes.

12. (Amended) The comparator unit of claim 11, wherein the first switch comprises an optically controllable switch.

29. (New) A comparator unit comprising:

a first amplifier stage including a differential amplifier having a pair of input nodes and a pair of output nodes including a first output node and a second output node, a non-linear load connected across the pair of output nodes, and a first switch connected between the first output node and a common node, a second switch connected between the second output node and the common node, and a third switch connected between the first output node and the second output node; and

a second amplifier stage coupled to the pair of output nodes.

30. (New) The comparator unit of claim 29, wherein the third switch comprises an electronically controllable switch.

31. (New) The comparator unit of claim 30, wherein the electronically controllable switch comprises an isolated gate field-effect transistor.

32. (New) The comparator unit of claim 29, wherein the non-linear load comprises a pair of cross-coupled isolated gate field-effect transistors.